Fast Viterbi Decoder IP-FV7P-C2

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ML-LABO

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Features

- VHDL IP Core
- Viterbi decoder of convolutional codes
- Code constraint length: k = 7
- Code rate: R = 1/2
- Path memory length: 48 bits
- Latency: 48+2 clocks
- Soft decision: 3bit (default)
- Architecture: Parallel
- Decoding Mode: Continuous
- Coding gain: 5.2dB @ BER = 10^{-5}
- Maximum clock frequency: 91MHz (on Xilinx XC2V1000-6)
- Maximum data rate: 91Mbps (on Xilinx XC2V1000-6)

Applications

- INMARSAT and INTELSAT
- Direct Broadcast Satellites (DVS)
- Wireless Data Links
- Very Small Aperture Terminal (VSAT)
- Digital Video Transmission System
- Military and Space Communication Systems

Table 1: IP-FV7P-C2 IP Core Facts

Design Parameters[1]	
Constraint Length	7
Code Rate	1 / 2
Code Generator G_0	171_8
Code Generator G_1	133_8
Soft Decision	3 bit
Path Memory Length	48 bit
Performance Characteristics	
Coding Gain	5.2dB @ BER=10^{-5}
Max. Clock Freq.[2]	91MHz
Data Rate [2]	91Mbps
Package Contents [3]	
Design Files	VHDL source
Verification	VHDL Test Bench
Documentation	User Manual
Option [4]	
Product Name: Fast Viterbi Decoder Design Kit Product Code: DK-FV7P-C2	

Notes:

1. The design parameters other than the constraint length and the number of generators can be customized.
2. The data is estimated on Xilinx XC2V1000-6.
3. All documents and files are shipped recorded in a CD-R.
4. If necessary, user can customize the core with this design kit. The design kit includes a tool for estimating BER and a tool for generating the test bench.

General Description

The Viterbi decoder is a forward error correction (FEC) decoder for covolutional codes used in various communication systems including INMARSAT, INTELSAT, DVS, and IEEE802.11.

The Viterbi decoder needs a large-scale hardware for searching a maximum likelihood path. So, it has been difficult to design high-speed Viterbi decoder with a small-scale hardware.

ML-LABO has invented a new algorithm for accelerating Viterbi decoder with a small-scale hardware. The IP-FV7P-C2 is accelerated by the algorithm, not by being optimized for Xilinx FPGA architecture. So, the IP-FV7P-C2 achieves an excellent performance even if it is implemented on ASIC.

Pinout

Figure1: IP-FV7P-C2 Pinout

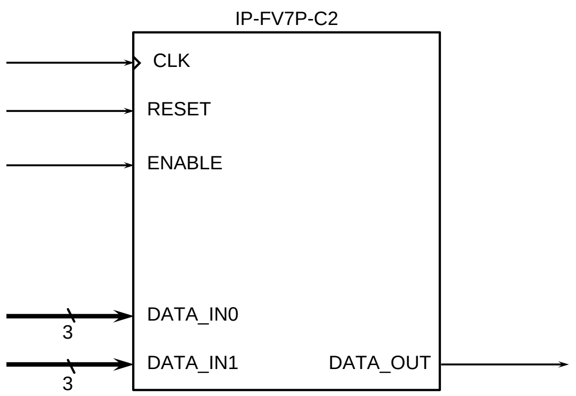


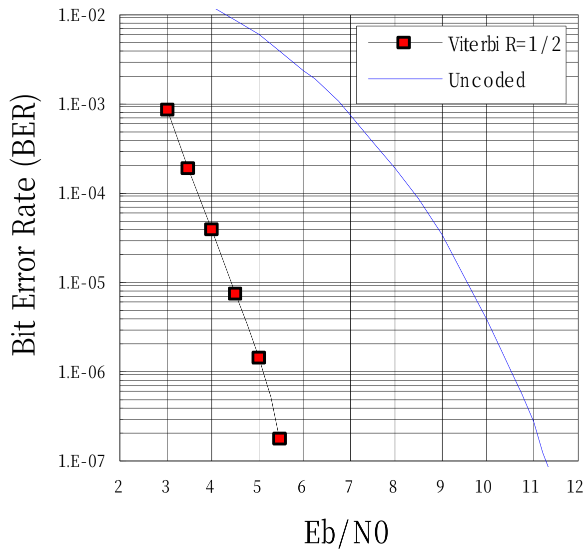
Table 2: IP-FV7P-C2 I/O Description

Signal	I/O	Description
CLK	I	System Clock
RESET	I	System Reset (Async.)
ENABLE	I	System Enable
DATA_IN0 DATA_IN1	I	Input buses, one for each output of the corresponding encoder. The width of the bus is 3 (default).
DATA_OUT	O	Output decoded data.

Bit Error Rate

The coding performance of IP-FV7P-C2 is shown in Figure 2. A coding gain of 5.2dB is achieved when operating at a decoded BER of 10^{-5}.

Figure 2: IP-FV7P-C2 BER



Performance Characteristics

The following performance and density characteristics have been obtained for the function implemented as a stand-alone design in the device specified bellow. If necessary, performance can be increased by selecting a device with a faster speed grade.

Table 3: Example IP-FV7P-C2 Implementation

Device	Xilinx XCV1000-6
Area (slices)	3,229
Equivalent Gates	73K
Latency	48+2 clocks
Maximum Clock Frequency	91MHz
Maximum Data Rate	91Mbps

Core Modifications

The design parameters other than the constraint length and the number of generators can be customized. ML-LABO provides core that is customized to user’s requirements.

The design parameters are implemented as a set of constants in a VHDL package file. So, if necessary, user can customize the core by himself. The corresponding test bench can be generated by the optional design kit DK-FV7P-C2.

Recommended Design Experience

Experience with convolutional encoding and the Viterbi decoding algorithm is recommended.